Version: 0.3
Total Pages: 27
Date: Aug. 9, 2005

Product Functional Specification

8.4 inch SVGA Color TFT LCD Module
Model Name: G084SN02
V0

( ) Preliminary Specification
(**u**) Final Specification

Note: This Specification is subject to change without notice.

I. Record of Revision

Version and Date	Page	Old Description	New Description	Remark
0.1 Mar/15/2005	All	First edition to customers	All	
0.2 Apr/18/2005	9; 23	Vibration level :1.0 G, Duration: X, Y, Z 120 min One time each direction	Vibration level :1.5 G, Duration: X, Y, Z 30 min One time each direction	
0.2 Apr/18/2005	25		Add label format	
0.3 Aug/8/2905	5	N/A	Add a discroption of RoHs model	

II. Contents

1.0 Handing Precautions

1) Front polarizer is fragile. Please be cautious and do not scratch it.
2) Be sure to turn off power supply when inserting to or disconnecting from input connector.
3) Wipe off water drop immediately. Long time water contact may cause discoloration or spots.
4) When panel surface is soiled, wipe it with absorbent cotton or soft cloth.
5) LCD panel is made of glass, it may be broken or cracked if it is dropped or bumped against hard surface.
6) Since CMOS LSI is used in this module, be cautious of static electricity and ensure human earth when handling.
7) Do not open nor modify the module assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case a TFT-LCD module has to be put back into the packing container slot once it's unpacked, do not press the center of the CCFL reflector edge. Instead, please press at the far ends of the CFL reflector edge softly. Otherwise the TFT module may be damaged.
10) Do not rotate nor tilt interface connector while inserting to or removing from the signal interface connector.
11) Do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT module from outside. Otherwise the TFT module may be damaged.
12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury corresponding with the RoHS directive. Please follow local ordinances or regulations for disposal.
13) The CFL in LCD module is designed for limited current circuit. Do not connect CFL in hazardous voltage circuit.

2.0 General Description

This specification applies to 8.4 inch color TFT LCD module G084SN02 V0.
This screen format supports SVGA (800(H) x 600(V)) screen and 262k colors (RGB 6-bits data driver).
All input signals are 1 channel LVDS interface compatible.
The module does not contain an inverter card for backlight.
This is an RoHs product.

Feature

This TFT LCD module complies with RoHS directive.
This is a 12 o'clock direction TFT LCD module.

Application

Internet Appliance (i.e. Tablet PC)

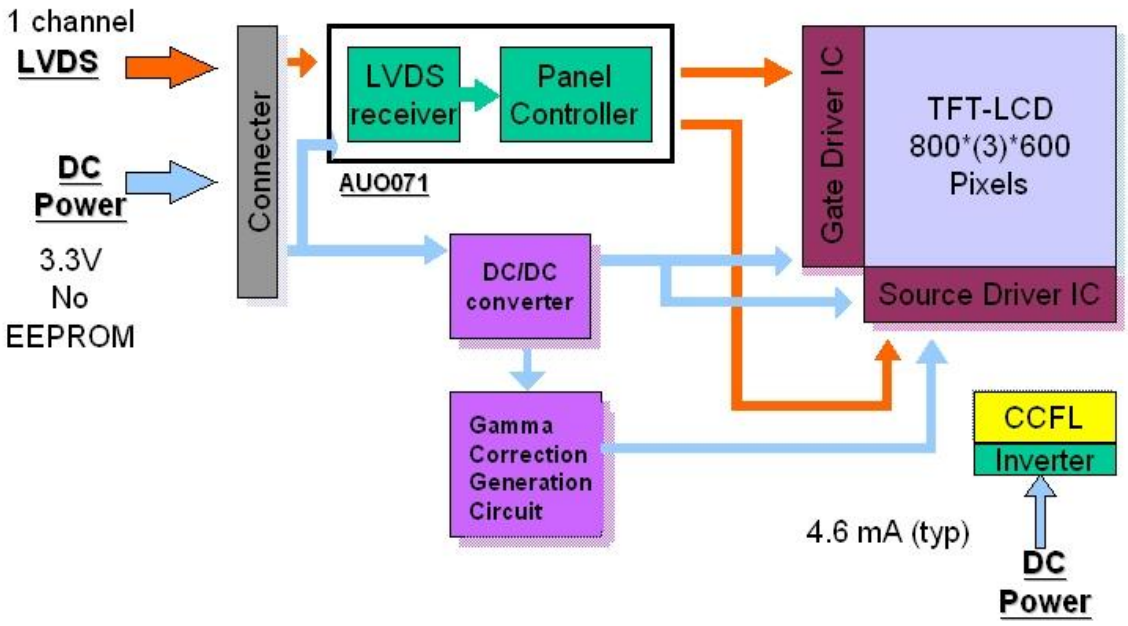
2.1 Display Characteristics

The following items are characteristic summary under 25℃ condition：

Items	Unit	Specifications
Screen Diagonal	[mm]	213.4 (8.4")
Active Area	[mm]	170.4(H) x 127.8(V)
Pixel H x V		800(x3) x 600
Pixel Pitch	[mm]	0.213(H) x 0.213(V)
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
Typical White Luminance (ICFL=4.6 mA)	[cd/m^2]	200 Typ. (center)
Contrast Ratio		500：1 Typ.
Optical Rise Time/Fall Time	[msec]	10/25 Typ.
Nominal Input Voltage VDD	[Volt]	3.3 Typ.
Typical Power Consumption (VDD line + VCFL line)	[Watt]	3.3 Typ (All Black Pattern)
Weight	[Grams]	210 ±10
Physical Size	[mm]	198.2(W) x 143.6(H) x 7.6(D) Max.
Electrical Interface		1 channel LVDS
Support Color		Native 262K colors (RGB 6-bit driver)
Temperature Range Operating Storage(Shipping)	 [℃] [℃]	 0 to +50 -20 to +60

2.2 Functional Block Diagram

The following diagram shows the functional block of the 8.4 inches Color TFT LCD Module：



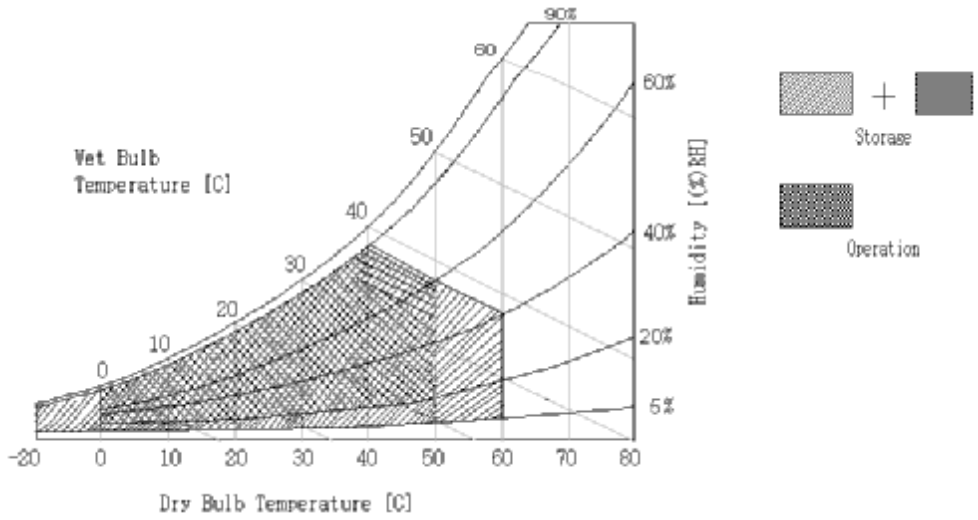
3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as follows：

Item	Symbol	Min	Typical	Max	Unit	Conditions
Logic/LCD Drive Voltage	VDD	3.0	3.3	3.6	[Volt]	
Input Voltage of Signal	Vin	3.3	3.6	3.9	[Volt]	
CCFL Current	ICFL	3	4.6	6	[mA] rms	
CCFL Ignition Voltage	Vs			820 (T=25℃)	Vrms	
Operating Temperature	TOP	0		+50	[℃]	Note1
Operating Humidity	HOP	5		90	[%RH]	Note1
Storage Temperature	TST	-20		+60	[℃]	Note1
Storage Humidity	HST	5		90	[%RH]	Note1
Vibration				1.5, 10-500	[G, Hz]	Sinusoidal wave 0.5hr/axis X,Y,Z
Shock				220, 2	[G, ms]	Half sine wave

Note: 1. Temperature and relative humidity range are shown in the figure below. Wet bulb temperature should be 39℃ and No condensation.

Wet bulb temperature chart

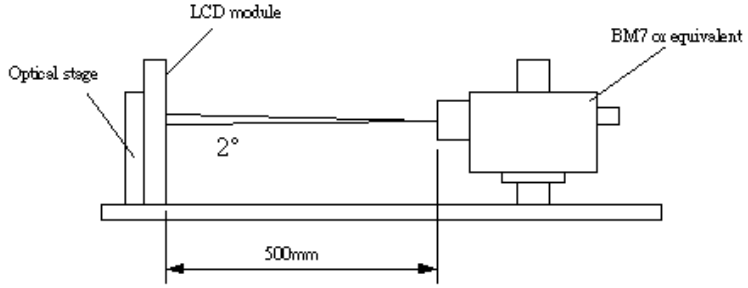


4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25 ℃ condition：

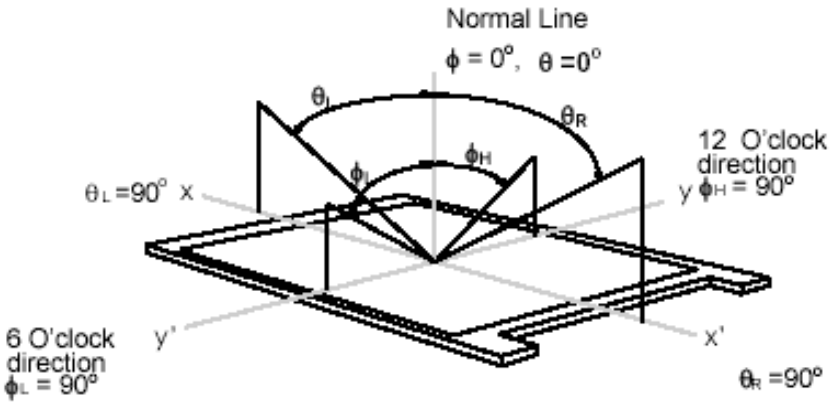
Item	Unit	Conditions	Min.	Typ.	Max.
Viewing Angle	[degree]	Horizontal (Right)	—	65	—
	[degree]	K = 10 (Left)		65	
K：Contrast ratio	[degree]	Vertical (Upper)	—	65	—
	[degree]	K = 10 (Lower)		45	
White Uniformity		9 Points	—	—	1.6
Contrast ratio		$\theta = 0^\circ$	—	500	—
Response Time	[msec]	Rising	—	10	20
(Room Temp)	[msec]	Falling	—	25	30
Color		Red x	0.540	0.570	0.600
Chromaticity		Red y	0.290	0.320	0.350
Coordinates(CIE)		Green x	0.290	0.320	0.350
		Green y	0.530	0.560	0.590
		Blue x	0.120	0.150	0.180
		Blue y	0.090	0.120	0.150
		White x	0.280	0.310	0.340
		White y	0.300	0.330	0.360
White Luminance	[cd/m^2]	$\theta = 0^\circ$	170	200	—
(ICFL 4.6 mA)					

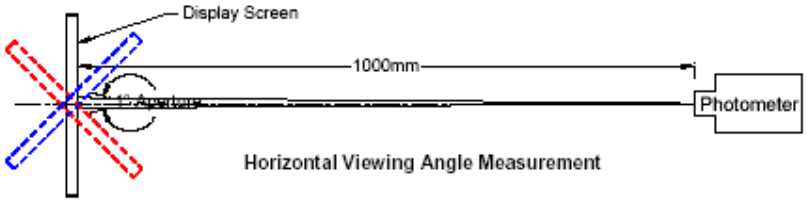
Optical characteristics are determined after the unit has been 'ON' and stable for approximately 30 minutes in a dark environment at 25℃. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and θ equal to 0°.

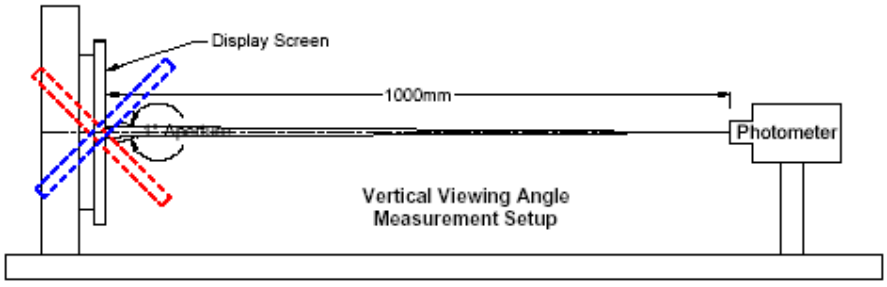


Note 1: Definition of Viewing Angle:

Viewing angle is the measurement of contrast ratio, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.





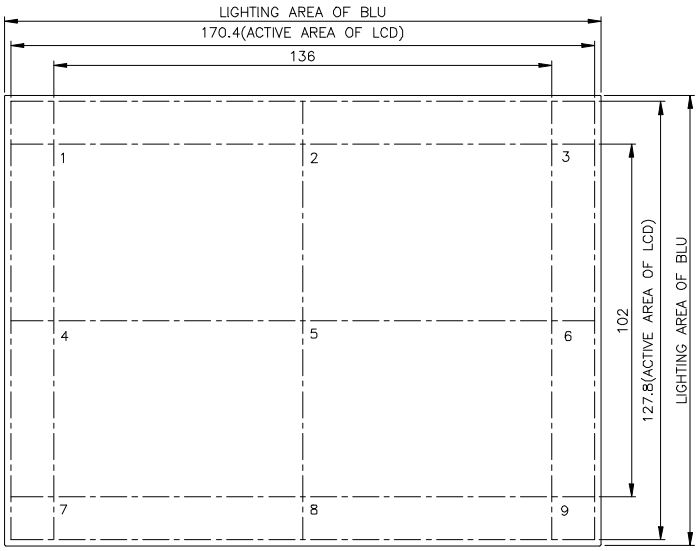


Note 2: Definition of white uniformity:

White uniformity is calculated with the following formula.

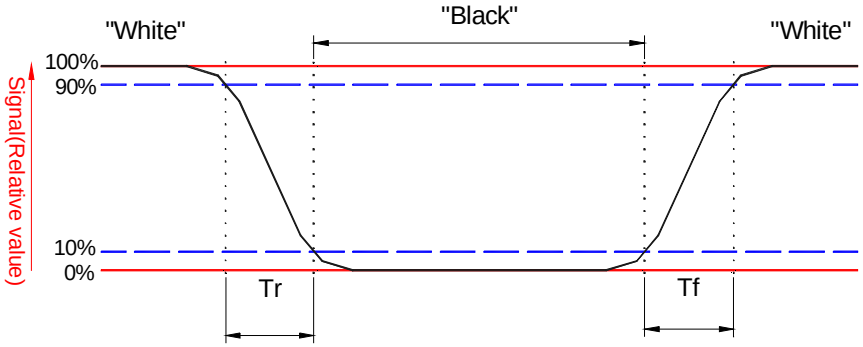
Luminance are measured at the following nine points (1~9).

$$\delta_W \frac{\text{Maximum Brightness of nine points}}{\text{Minimum Brightness of nine points}}$$



Note 3: Definition of response time:

The output signals of photo-detector are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	HIROSE
Type / Part Number	HRS DF 19K series
Mating Connector / Part Number	DF19G-20S-1C (WIRE TYPE) or competiable
Mating Connector / Part Number	DF19-20S-1F (FPC TYPE) or competiable

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1 or competiable
Mating Connector / Part Number	SM02B-BHSS-1-TB or competiable

5.2 Signal Pin – LVDS Connector

Pin No.	Signal Name	Pin No.	Signal Name
1	VDD	2	VDD
3	GND	4	GND
5	RxIN0-	6	RxIN0+
7	GND	8	RxIN1-
9	RxIN1+	10	GND
11	RxIN2-	12	RxIN2+
13	GND	14	RxCKIN-
15	RxCKIN+	16	GND
17	NC	18	NC
19	GND	20	GND

5.3 Signal Pin - Lamp connector

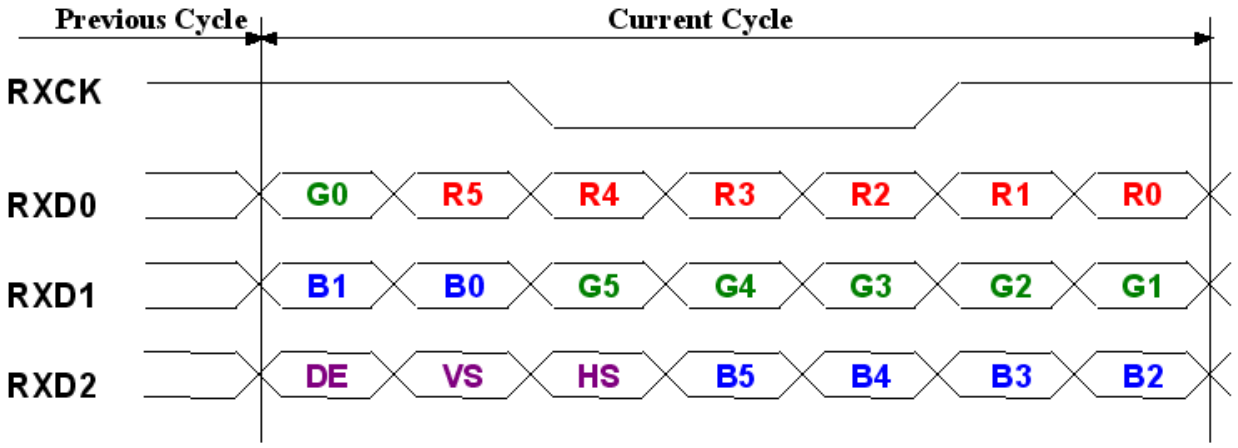
Pin no.	Symbol	Function	Remark
1	H	CCFL power supply(H.V.)	Cable color: Pink
2	L	CCFL power supply(GND)	Cable color: White

5.4 Signal Description

The module uses a LVDS receiver. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS84 (negative edge sampling) or compatible.

Note： Input signals shall be in low status or Hi-Z state when VDD is off.

Signal Name	Description
RxIN0-, RxIN0+	LVDS differential data input (Red0-Red5, Green0)
RxIN1-, RxIN1+	LVDS differential data input (Green1-Green5, Blue0-Blue1)
RxIN2-, RxIN2+	LVDS differential data input (Blue2-Blue5, Hsync, Vsync, DE)
RxCKIN-, RxCKIN+	LVDS differential clock input
VDD	+3.3V Power Supply
GND	Ground
NC	No Connection



Signal Name	Description	
+RED5 +RED4 +RED3 +RED2 +RED1 +RED0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
+GREEN5 +GREEN4 +GREEN3 +GREEN2 +GREEN1 +GREEN0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
+BLUE5 +BLUE4 +BLUE3 +BLUE2 +BLUE1 +BLUE0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
CLK	Data Clock	The typical frequency is 40MHz. The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of CLK. When the signal is high, the pixel data shall be valid to be displayed.
VSYNC	Vertical Sync	The signal is synchronized to CLK.
HSYNC	Horizontal Sync	The signal is synchronized to CLK.

Note：Output signals from any system shall be low or Hi-Z state when VDD is off.

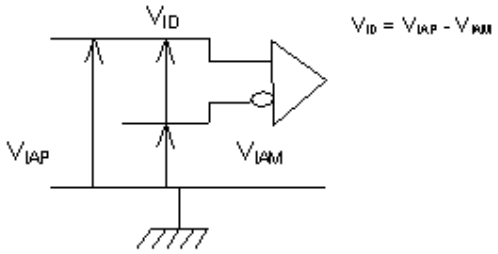
5.5 Signal Electrical Characteristics

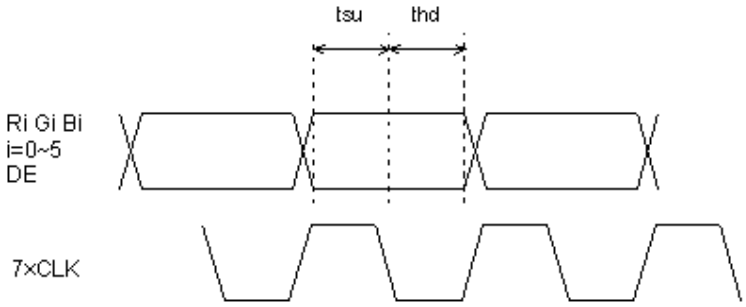
Input signals shall be low or Hi-Z state when VDD is off.

It is recommended to refer the specifications of SN75LVDS86(Texas Instruments) in detail.

Signal electrical characteristics are as follows：

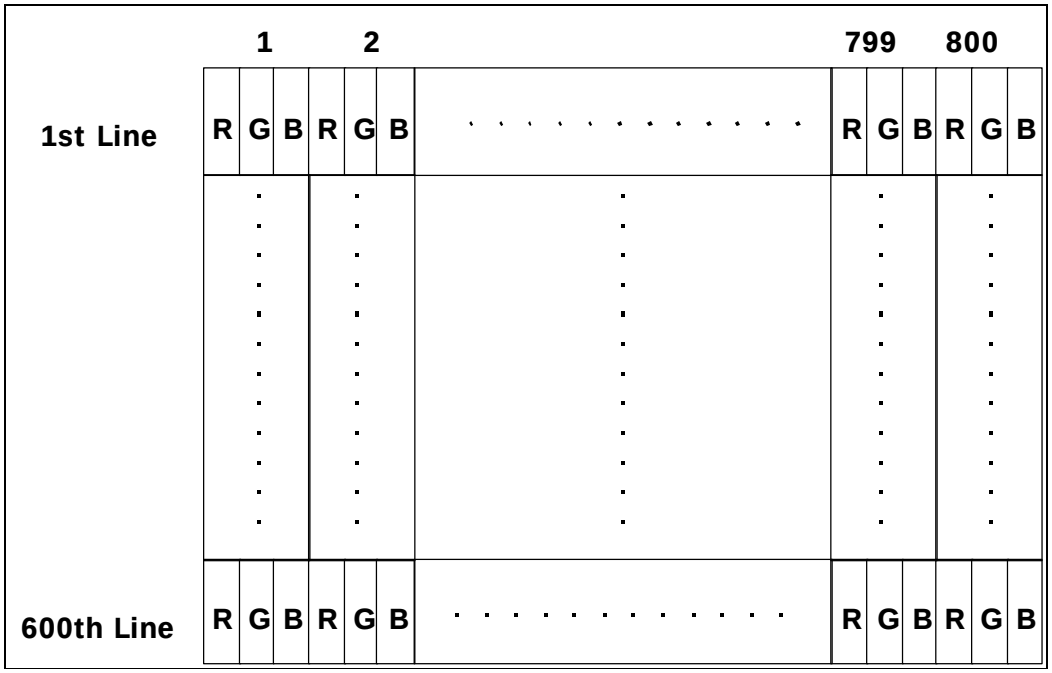
Item	Symbol	Min.	Typ.	Max.	Unit
The differential level	| VID |	0.1	-	0.6	V
The common mode input voltage	VIC	$\frac{\lvert VID \rvert}{2}$	-	$2.4 - \frac{\lvert VID \rvert}{2}$	V
The input setup time	tsu	0.5	-	-	ns
The input hold time	thd	0.5	-	-	ns
High-level input voltage	V_{IAP}	2.0			V
Low-level input voltage	V_{IAM}			0.8	V
Clock frequency	CLK	38	40	48	MHz





6.0 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format：



7.0 Parameter guide line for CFL inverter

Parameter	Min	Typ	Max	Units	Condition
White Luminance	170	200	-	Cd/m^2	
CCFL current (ICFL)	3.0	4.6	6.0	mArms	Note1
CCFL Frequency (FCFL)	50	60	80	KHz	Note4
CCFL Ignition Voltage (Vs)	-	-	1070(T=0℃) 820(T=25℃)	Vrms	Note3
CCFL Voltage (Reference) (VCFL)	441	490	539	Vrms	Note1
CCFL Power consumption (PCFL)	-	2.3	-	W	Note2
Lamp Life Time	10,000	20,000	-	Hr	Note1, 5

Note1：T=25℃

Note2：Inverter should be designed with the characteristic of lamp. When you are designing the inverter, the output voltage of the inverter should comply with the following conditions.

(1). The area under the positive and negative cycles of the waveform of the lamp current and lamp voltage should be area symmetric (the symmetric ratio should be larger than 90%).

(2). There should not be any spikes in the waveform.

(3). The waveform should be sine wave as possible.

(4). Lamp current should not exceed the maximum value within the operating temperature (It is prohibited to over the maximum lamp current even if operated in the non-guaranteed temperature). When lamp current is over the maximum value for a long time, it may cause fire. Therefore, it is recommend that the inverter should have the current limit circuit.

Note3：The inverter open voltage should be designed larger than the lamp starting voltage at $T=0^oC$, otherwise backlight may be blinking for a moment after turning on or not be able to turn on. The open voltage should be measured after ballast capacitor. If an inverter has shutdown function it should keep its open voltage for longer than 1 second even if lamp connector is open.

Note4：Lamp frequency may produce interference with horizontal synchronous frequency and this may cause line flow on the display. Therefore lamp frequency shall be detached from the horizontal synchronous frequency and its harmonics as far as possible in order to avoid interference.

Note5：Brightness (ICFL=4.6mA) to be decreased to the 50% of the initial value.

8.0 Interface Timings

Basically, interface timing should match the VESA 800x600 /60Hz(VG901101) manufacturing guide line timing.

8.1 Timing Characteristics

(a) DE mode

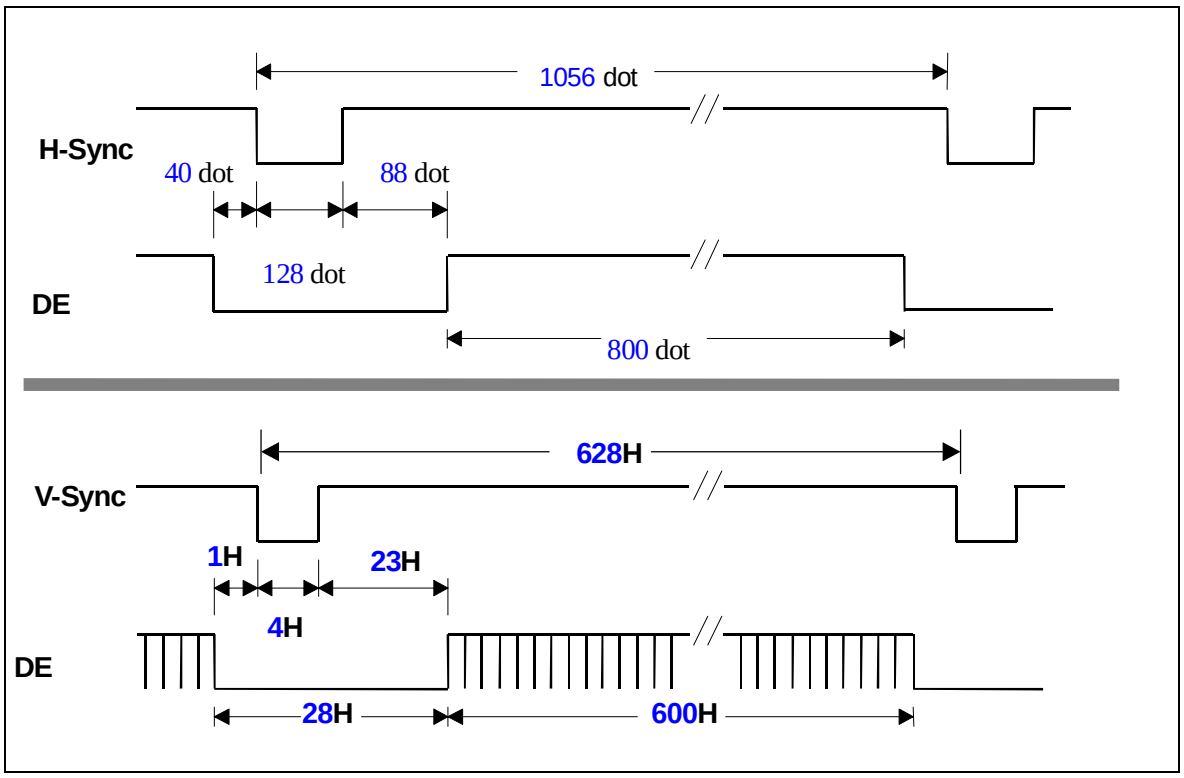
Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Clock frequency	Fck	38	40	48	MHz	
Horizontal blanking	Thb1	50	256	500	Clk	
Vertical blanking	Tvb1	10	28	150	Th	

(b) HV mode

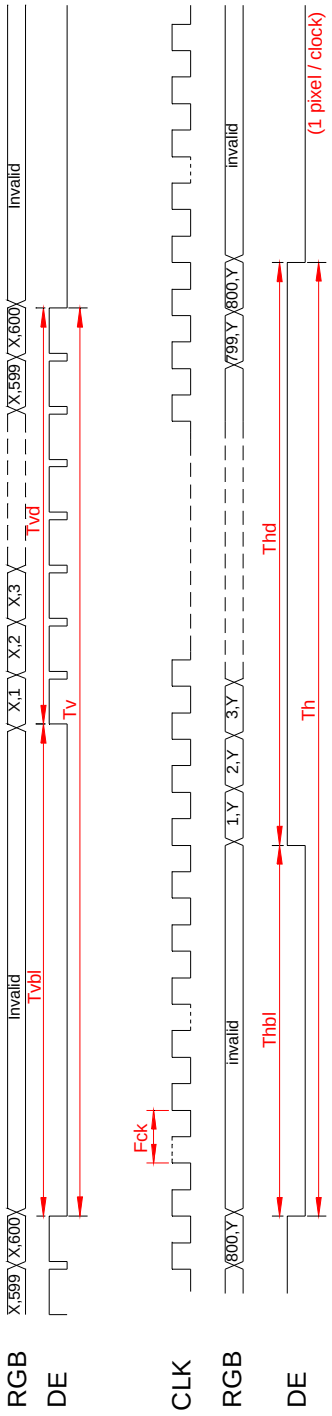
Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Clock frequency	Fck	38	40	48	MHz	
Hsync period	Th	850	1056	1300	Clk	
Hsync pulse width	Thw	10	128	-	Clk	
Hsync front porch	Thf	15	40	-	Clk	
Hsync back porch	Thb	10	88	-	Clk	
Hsync blanking	Thb1	50	256	500	Clk	
Vsync period	Tv	610	628	750	Th	
Vsync pulse width	Tvw	1	4	-	Th	
Vsync front porch	Tvf	0	1	-	Th	
Vsync blanking	Tvb1	10	28	150	Th	
Hsync/Vsync phase shift	Tvpd	2	320	-	Clk	

Item	Symbol	Value	Unit	Description
Horizontal display start	The	218	Clk	After falling edge of Hsync, counting 218clk, then getting valid data from 219th clk's data.
Vertical display start	Tve	25	Th	After falling edge of Vsync, counting 25th, then getting 26th Th's data.

8.2 Timing Definition



Timing Chart

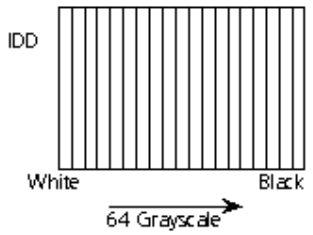


9.0 Power Consumption

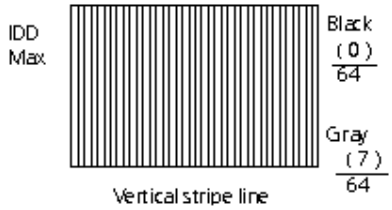
Input power specifications are as follows：

Symbol	Parameter	Min	Typ	Max	Units	Condition
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	V	
PDD	VDD Power	-	0.76	-	W	
PDD Max	VDD Power max	-	0.86	-	W	
IDD	IDD Current	-	230	-	mArms	Note 1
IDD Max	IDD Current max	-	260	310	mArms	Note 2
V_{RP}	Power Ripple Voltage	-	100	-	mVp-p	
I_{RUSH}	Inrush Current	-	1500	-	mApeak	

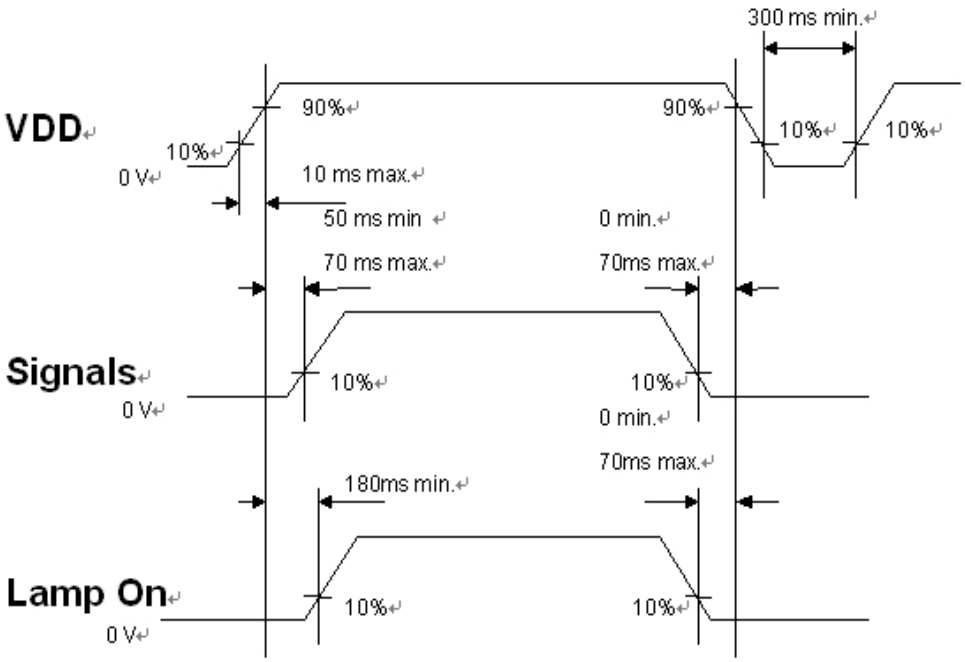
Note 1: Effective value (mArms) at V_{CC} = 3.3 V/25℃.



Note 2:



10.0 Power ON/OFF Sequence



VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.

11.0 Reliability Test Items

Environment test condition

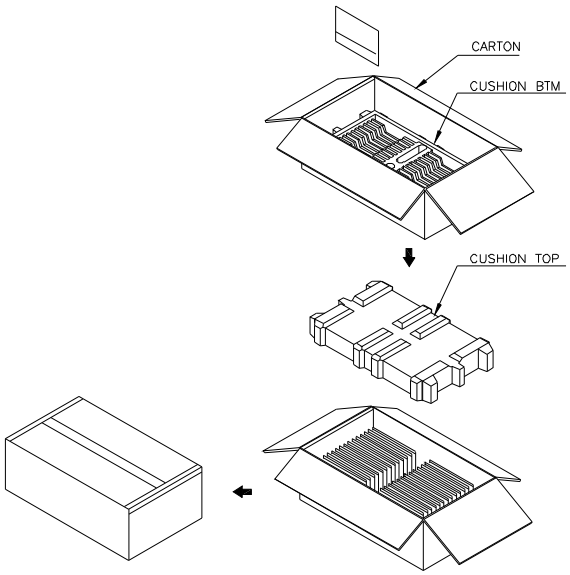
No	Test Item	Condition	Remark
1	High temperature storage test	Ta=60℃ 300Hrs	Note 1,2,3
2	Low temperature storage test	Ta= -20℃ 300Hrs	Note 1,2,3
3	High temperature operation test	Ta=50℃ 300Hrs	Note 1,2,3
4	Low temperature operation test	Ta=0℃ 300Hrs	Note 1,2,3
5	High temperature & high humidity operation	40℃, 90%RH, 300Hrs (No condensation)	Note 1,2,3
6	Thermal Shock Test (non-operation)	-20℃/30 min, 60℃/30 min 100cycles	Note 1,2,3
7	Vibration test (non-operation)	Vibration level :1.5 G Waveform: Sinusoidal vibration Bandwidth : 10-500-10Hz/2.5min Duration: X, Y, Z 30min One time each direction	Note 1,2,3
8	Shock test (non-operation)	Shock level: 220G Waveform: Half sine wave, 2ms Direction: ±X, ±Y, ±Z One time each direction	Note 1,2,3
9	Electrostatic discharge (non-operation)	150 pF,150Ω,10kV,1 second, 9 position on the panel, 10 times each place	Note 3

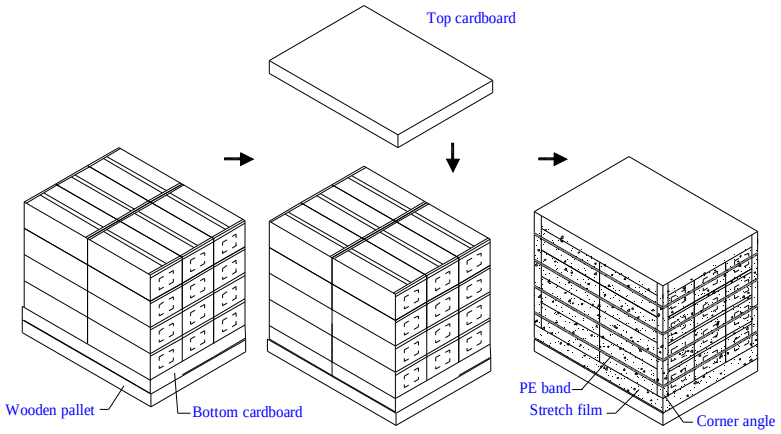
Note 1: Evaluation should be tested after storage at room temperature for one hour.

Note 2: There should be no change which might affect the practical display function when the display quality test is conducted under normal operating condition.

Note 3: Judgment: Function and display OK.

12.0 Packing





Note : Limit of box palletizing = Max 4 layers(ship and stock conditions)

Note:

1. Maximun Capacity: 30 LCD Module Carton
2. Carton outside dimension: 600 (L)mm x 353 (W)mm x 210 (H)mm
3. Maximun 24 of corrugated carton on wooden pallet.
   (3 x 2 x 4 layers : maximun 24 boxes per pallet: 720 pcs modules)

12.1 Label format

13.0 Mechanical Drawings